CLAIMS

1. An apparatus to allow dual master control of a slave peripheral unit, comprising:

a first and a second master control unit, each master control unit able to provide control bits;

a slave peripheral unit operable by a shared subset of the control bits from the master control units;

a slave peripheral interface coupled between the master control units and the slave peripheral unit, the interface includes a data communication bus for carrying the control bits; and

a logic configuration block coupled to the communication bus, the logic configuration block controls access of the shared subset of control bits to the slave peripheral unit, the block configurable by a set of configuration bits accessible by only a first master control unit.

2. The apparatus of claim 1, wherein the configuration bits set logic configuration bits in the logic configuration block, the logic configuration bits defining the control of the common subset of shared control bits by the master control units.

3. The apparatus of claim 1, wherein the configuration bits set a logic operation in the logic configuration block, the logic operation operates on the shared control bits from the master control units to define a combined output set of control bits to control the peripheral.

4. The apparatus of claim 1, wherein the slave peripheral unit includes respective first and second input registers coupled to the first and second master control units through the communication bus, the input registers being coupled to provide the shared control bits from the master control units to the logic configuration block, and wherein the slave peripheral unit includes a configuration register accessible to the first master control unit and coupled to provide configuration bits to the logic configuration block.

5. The apparatus of claim 4, wherein the second main control unit is operable to read the configuration register to confirm accessibility of the slave peripheral unit by the second main control unit.

6. The apparatus of claim 4, wherein the slave peripheral unit includes an output to output the logical combination of the shared control bits of the master control units from the logic configuration block.

7. The apparatus of claim 6, wherein the output is coupled to the shift registers to output data back to the respective master control units.

8. The apparatus of claim 6, wherein the second main control unit is operable to read the output to confirm operability of the slave peripheral unit by the second main control unit.

9. An apparatus to allow dual master control of a slave peripheral unit, comprising:

a first and a second master control unit, each master control unit able to provide control bits;

a slave peripheral unit operable by a shared subset of the control bits from the master control units, the slave peripheral unit includes respective first and second input registers that receive the control bits from master control units and a configuration register accessible by the first master control unit;

a slave peripheral interface including a data communication bus coupled between the control units and the respective input registers of the slave peripheral unit, the communication bus for carrying the control bits; and

a logic configuration block coupled to the input registers and the configuration register, the logic configuration block controls access of the shared subset of control bits to the slave peripheral unit, the block configurable by a set of configuration bits from the configuration register.

10. The apparatus of claim 9, wherein the configuration bits set a logic operation in the logic configuration block, the logic operation operates on the shared control bits from the master control units to define a combined output set of control bits to control the peripheral.

11. The apparatus of claim 9, wherein the second main control unit is operable to read the configuration register to confirm accessibility of the slave peripheral unit by the second main control unit.

12. The apparatus of claim 9, wherein the slave peripheral unit includes a output to output the logical combination of the shared control bits of the master control units from the logic configuration block, and wherein the second main control unit is operable to read the output to confirm operability of the slave peripheral unit by the second main control unit.

13. The apparatus of claim 9, wherein the communication bus is a serial communication bus.

14. A method of providing dual master control of a slave peripheral unit, the method comprising the steps of:

providing a first set of control bits and a set of logic configuration bits from a first master control unit, and providing a second set of control bits from a second master control unit;

configuring a logic operation in a combinational logic block with the set of logic configuration bits;

performing the logical operation on the first and second set of control bits to provide a resultant set of control bits; and

applying the resultant control bits to a slave peripheral unit.

15. The method of claim 14, further comprising the step of reading the configuration bits by the second master unit to confirm accessibility of the slave peripheral unit.

16. The method of claim 14, further comprising the step of reading the resultant control bits by the second master unit to confirm operability of the slave peripheral unit.

17. The method of claim 14, wherein the providing step includes providing the control bits serially in a common format.